

App. No. 10/809,215
Office Action Dated March 10, 2006

REMARKS

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claims 2, 3, 10, and 12 are hereby amended. Amendments of claims 2, 3, 10, and 12 are supported by page 9, lines 22-32 and Figure 11.

Claims 2-9 were rejected as being unpatentable over Yuzurihara (EP 1075028) in view of Maeda (US 6,492,668). Applicants traverse this rejection. The combination of Yuzurihara and Maeda does not suggest a solid-state imaging apparatus including a floating diffusion layer that is exposed on the surface of a semiconductor substrate in a region other than a periphery of a contact portion of the floating diffusion layer, while a region within the periphery of the contact portion is covered with a salicide layer, wherein an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of either the amplifier transistor or a plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit, as required respectively by claims 2 and 3. The rejection relies on Maeda to teach an impurity concentration of the floating diffusion layer that is lower than that of the source/drain diffusion layer. While Maeda may teach a source/drain region of a MOS transistor having a low concentration diffusion layer (4a) for suppressing leakage current, and another source/drain region having a high concentration diffusion layer (4b), Maeda fails to suggest a low diffusion concentration floating diffusion layer that is exposed on a surface of a semiconductor substrate in a region other than a periphery of a contact portion of the floating diffusion layer, while a region within the periphery of the contact portion is covered with a salicide layer.

The low diffusion concentration required by claims 2 and 3 provides a solid-state imaging apparatus in which an increase of contact resistance is effectively suppressed, thereby efficiently outputting a charge signal from an amplifier transistor. The contact portion of the floating diffusion layer is connected with a gate electrode of the amplifier transistor. A signal charge generated in the photodiode and accumulated temporarily in the floating diffusion layer is amplified by the amplifier transistor through the contact portion and output. Therefore, it is desirable for the contact resistance of the contact portion to be low. However, in a

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configuration, such as that taught by Maeda, in which the impurity concentration of the floating diffusion layer is made low so as to suppress leakage current, a contact resistance of the contact portion becomes high compared with a conventional floating diffusion layer with a high impurity concentration, thereby causing a signal charge to be insufficiently output. The low impurity concentration of the floating diffusion layer required by claim 2 and 3, along with the requirement that the floating diffusion layer is not covered with the salicide layer (so as to be exposed on a surface of the semiconductor substrate) provides a reduced pn-junction opposite-direction leakage current in the floating diffusion layer. As a result, a solid-state imaging apparatus with low noise and high sensitivity is provided.

Favorable reconsideration of claims 2-9 is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612)455-3804.

Dated: June 6, 2006



DPM:mfe

Respectfully Submitted,

A handwritten signature in black ink, appearing to be "D. Mueller", written over a horizontal line.

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